# A 155-GHz Monolithic Low Noise Amplifier

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## ABSTRACT

This paper presents the design, fabrication and performance of a three-stage 155-GHz monolithic low noise amplifier (LNA) using 0.1 -μm pseudomorphic (PM) InAlAs/InGaAs/InP HEMT technology. This amplifier exhibits a measured small signal gain of 12 dB at 155 GHz, and more than 10 dB gain from 151 to 156 GHz. When this amplifier is biased for low noise figure, a noise figure of 5.1 dB with associated gain of "IO. 1 dB is achieved. Besides its excellent noise performance, this is the highest frequency amplifier ever reported using three terminal devices.

## I. INTRODUCTION

Millimeter-wave (MMW) LNA's are very important components for smart -- munitions, passive imaging and radiometer applications. The PM HEMT devices using both GaAs and InP materials have demonstrated the high gain and low noise capability at W-band (75- 110 GHz) and D-band (110-170 GHz) frequencies for hybrid integrated circuits [1 ]-[2]. High gain low noise amplifiers have been successfully developed up to 140 GHz [3]-[6], as referred in the summary of previously published InP-based HEMT MMIC LNA results listed in [12]. For the frequency range above 120 GHz, InP-based HEMTs are superior to GaAs-based HEMT's for amplification due to the higher electron

peak drift velocity in the InP based HEMT devices. The MMIC LNA's fabricated using the InP HEMT MMIC process have also achieved state-of-the-art high gain and low noise figure performance at lower frequencies. Examples include a Q-band (44.5 GHz) two-stage balanced LNA exhibiting 2.2-dB noise figure with 20-dB associated gain [7], and a W-band four-stage balanced amplifier with a small signal gain of 23 dB from 75 to I IO GHz [8]. A two-stage cryogenically cooled W-band LNA also exhibited 0.7-dB NF at 95 GHz with 12-dB associated gain [9]. The motivation of this work is to push the state-of-the-art and demonstrate higher frequency performance in a monolithic LNA to 155 GHz using the 0.1 -μm passivated InP-based HEMT MMIC technology [1 1].

This paper presents the design, fabrication and testing of a 155-GHz monolithic three-stage amplifier using 0.1 -μm InAlAs/InGaAs/InP PM HEMT technology. A measured small signal gain of 12 dB is achieved at 155 GHz. When this LNA is biased for low noise figure, 5.1 -dB noise figure with 10.1 -dB gain is obtained. To our knowledge, this is the highest frequency amplifier ever reported using three terminal devices and represents the state-of-the-art in low noise performance of InP HEMT MMIC LNAs.

## II. DEVICE FABRICATION AND CHARACTERISTICS

The three-stage 155-GHz MMIC LNA chip was fabricated on a 2" Fe-doped semi-insulating InP substrate grown by molecular beam epitaxy and employs 0.1 -μm T-gate InP HEMT devices. The InAlAs/InGaAs/InP HEMT ($In_{0.65}Ga_{0.35}As$ channel) structure InP HEMT MMIC process follows the procedures reported in [2], with additional wafer passivation and stabilization bake steps introduced to the MMIC process [1 1]. Fig. 1 shows the InP HEMT device layer structure. The channel is a 150 A pseudomorphic 65% Iridium composition InGaAs layer which provides superior transport properties and high electron sheet densities. Typical room temperature Hall mobility of 10500-11000 $cm^2/V$-sec and Hall sheet carrier concentration of 3.5x $10^{12}/cm^2$ are measured on undoped cap layer _. calibration samples.

The devices are isolated using a combination wet etch/boron implantation process which provides better than 10 MΩ/square resistance. Source and drain Ni/Au-Ge/Ag/Au ohmic contacts alloyed at 400°C using rapid thermal annealing, provide a very low ohmic contact resistance of 0.06 Ω-mm and a source resistance of 0.2 Ω-mm. The 0.1 -μm gate stripes are fabricated with a hi-layer PMMA/PMMA-MAA resist profile for metal liftoff and

are offset 0.6 μm from the source pad. Prior to metalization, the devices are gate recess etched to a predetermined current level. The target device pinchoff voltage of -0.25 V with the voltage at a peak transconductance ($V_{gp}$) of 1000 mS/mm, are attained with a unity current gain frequency ($f_T$) of 200 GHz, and a maximum oscillation frequency ($f_{max}$) of 400 GHz. Device reverse breakdown voltage, defined at 0.2 and 1.0 mA/mm reverse gate leakage current, are 1.5 and 2.5 V, respectively. The devices are passivated with 750 A silicon nitride deposited using PECVD. For the MMIC process, precision NiCr resistors with a target resistance of 100 Ω/square and silicon nitride MIM capacitors with a target sheet capacitance of 300 pF/mm$^2$ are used. After front side processing, the wafers are lapped and polished to 75 μm thickness. Ground via holes are wet-chemical etched and 3.5-pm gold is plated on the back side of the wafers to complete the MMIC process.

## III. DEVICE MODELING AND CIRCUIT DESIGN

The linear small signal model for a 0.1 -μm gate PM InP HEMT, used in this 155-GHz LNA design, was obtained from curve fitting of the measured transistor small signal S-parameters up to 50 GHz. The resulting equivalent circuit parameters are consistent with the estimated values based on device physical dimensions and electrical/process parameters.

Fig. 2(a) shows the schematic diagram of this monolithic amplifier and Fig. 2(b) contains a chip photograph of the 2.5 mm x 1.6 mm chip. The 155-GHz amplifier is a ‘three-stage single-ended design. Each stage uses a 30-pm PM InP HEMT device for a lower gate resistance and gate-drain capacitance so as to have higher device gain at the frequency, The circuit design utilizes a similar quasi-low-pass topology in the matching structures as that used in the previously published 140-GHz MMIC LNA [6]. This simple matching topology was chosen to minimize the uncertainties in the analysis and modeling at such a high frequency and thus reduce the design risk. The input, output and inter-stage matching networks are all constructed by cascading high-low impedance microstrip lines on a 75-μm thick InP substrate to maximize the gain performance. Edge coupled lines are used for dc blocking and radial stubs are employed for RF bypass. Shunt RC networks are included in the bias circuitry to maintain amplifier stability. A wet chemical etching process is used to fabricate back side via holes for grounding. The design and analysis procedures of the monolithic chip design, which include accurate active device modeling and full-wave electromagnetic (EM) analysis of passive structures, is documented in [10].

## IV. TRANSITION AND TEST-FIXTURE DESIGN

For testing, the InP amplifier chip is coupled to WR-5 waveguide at the input and output through a quartz E-plane probe structure. The probe was designed by utilizing a waveguide-to-microstrip cross junction structure, similar to designs at lower frequencies (26 to 110 GHz) [13]. A full-wave electromagnetic analysis software package, HFSS [14], was used for the design. A schematic is given in Fig. 3 along with transition dimensions. The transition consists of a printed microstrip-line circuit on 0.003" thick fused quartz, a portion of which extends into the WR5 (140-220 GHz) waveguide through an aperture in the broad wall. The width of the quartz substrate is chosen to eliminate waveguide modes in the microstrip cavity. In order to have a low insertion loss and to be insensitive to mechanical alignment error between the probe and the waveguide, the probe sectional lengths (D 1 and D2), widths (W 1 and W2), and the back-short location (L) are designed to have relatively large values. The critical dimensions of the transition are given in the figure caption.

A photo of the transition (back-to-back) is given in Fig. 4(a). For determining the transition 1oss and match, two fixtures are connected back-to-back with a 0.130' long, 0.006" wide microstrip line joining the waveguide. The measured frequency response from 144 to 170 GHz is shown in Fig. 4(b). The insertion loss for a pair of back-to-back transitions was approximately 2.5 dB and the return loss measured about 15 dB from 152 to 168 GHz.

## V. AMPLIFIER MEASUREMENT

The 155-GHz LNA chip was mounted and tested in the G-band (WR5, 140-220 GHz) waveguide fixture described in Section IV. The complete fixture, with the MMIC chip mounted, is shown in the photograph in Fig. 5. The amplifier gain and return were measured with a scalar test system based around a 120-170 GHz sweepable backward wave oscillator. A block diagram of the measurement set up is shown in Fig. 6. A series of reference sweeps were taken using a calibrated attenuator, and the MMIC LNA chip mount was then inserted in order to measure the gain and insertion loss. Fig. 7 shows the gain and input/output return loss from 144 to 170 GHz. A peak gain of 12 dB occurs between 153-155 GHz and the amplifier demonstrates more than 10 dB gain from 151 to 156 GHz. The input and output return loss are better than 5 and 10 dB, respectively. The gain curve refers to the chip and has had 2.5 dB added to account for the transition loss.

The total dc power consumption for this achieved gain is only 35 mW ($V_d$ = 1.4 V, $I_{total}$ = 25 mA). The gain compression effect is also investigated under different input power levels. Fig. 8 shows the output power and gain at three input power levels under identical bias conditions at 155 GHz. As can be observed, the power gain of this amplifier was compressed by about 1.5 dB when the input power was increased from -9 to -4 dBm.

The spot noise temperature of the amplifier was measured with a calibrated noise test system normally used to measure waveguide mixers. A block diagram appears in Fig. 9. The system was calibrated using room-temperature and liquid nitrogen loads at the input horn of a subharmonically pumped planar-Schottky-diode mixer with a double side-band noise temperature between 2000 and 3000K. The IF test system is precalibrated to read noise power in degrees using room temperature and 77K coaxial loads. The reference plane for the test set is the end of the IF cable which attaches to the output port of the mixer. During measurements, the mixer noise and conversion loss (Reference Noise Temperature in the figure) are determined by placing the hot and cold black body loads at the input of the WR5 horn attached to the mixer input RF port. The horn is then moved to the output port of the amplifier and the measurement is repeated. Ignoring amplifier output mismatch, the gain and noise of the amplifier *is* simply given by:

$$G_{amp}(dB) = L_{mixer} + L_{mixer+amp},$$

$$T_{amp} = T_{mixer+amp} - T_{mixer}/G_{amp}.$$

The amplifier noise figure is then

$$NF(dB) = 10 \log(T_{amp}/290+1).$$

The amplifier was then inserted between the mixer and horn and the de-embedded loss (now gain) and excess input noise temperature were backed out of the measured response. No correction for amplifier-to-mixer mismatch was made. The gain and noise - were measured at three representative frequencies: 150, 155 and 160 GHz. The output - intermediate frequency was fixed at 1.5 GHz and the pre-detection bandwidth for the spot noise measurement was 10 MHz. The results, accounting for 2.5-dB of transition loss under a drain voltage of 1.4 V with each stage drawing 10-mA current are plotted in Fig. 10. A measured noise figure of 6.8 dB with associated small signal gain of 11 dB is achieved at 155 GHz. Two amplifiers were measured, with one of the chips having approximately 1 dB lower noise figure than the other. Optimum bias conditions for

minimum noise turned out to be 1.4 V drain bias for all three stages with 3, 5 and 7 mA of current for stages 1, 2 and 3, respectively. Under these conditions, from flange to flange, 6.4-dB noise figure (964 K) with 7.6-dB associated gain (noise figure of 5.1 dB, and 10.1 -dB gain at the chip assuming 1.25-dB loss per transition) is obtained, as shown in Table 2. This is believed to be the best reported performance for an amplifier at this frequency and the first measurements of amplifier noise above 140 GHz.

## VI. SUMMARY

We have described the design, structure and measurements of a 155-GHz monolithic low noise amplifier using 0.1 -μm PM InGaAs/InAlAs/InP HEMT technology. The three-stage single-ended 155-GHz monolithic LNA exhibits a small signal gain of 12 dB at 155 GHz, and more than 10 dB of gain from 151 to 156 GHz. A noise figure of 5.1 dB with 10.1 -dB associated is also achieved under a low current bias condition at 155 GHz. To the best of our knowledge, this is the highest frequency amplifier ever reported using three terminal devices.

## ACKNOWLEDGMENT

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## FIGURE CAPTIONS

Fig. 1. InGaAs/InAlAs/InP PM HEMT device layer structure.

Fig. 2. (a) Circuit schematic diagram, and (b) chip photograph of the 155-GHz InP-based HEMT MMIC low noise amplifier.

Fig. 3. (a) Three dimensional view of the waveguide to microstrip-line transition. (b) Top view of the microstrip line, D 1 = 0.011 ", W1 = 0.03", D2 = 0.007", W2 = 0.006", L = 0.0185".

Fig. 4. (a) Photograph of the transition test-fixture, and (b) measured through insertion loss and return loss between 140 and 175 GHz.

Fig. 5. Photograph of the 155-GHz MMIC LNA mounted in the transition test-fixture.

Fig. 6. Block diagram of the scalar test system for measuring amplifier gain. The calibrated attenuator is used to set the reference gain levels. The variable attenuator is used for detector matching. All unlabeled waveguideisWR6(110-170 GHz).

Fig. 7. Measured small signal gain (referred to the chip) and return loss of the 155-GHz MMIC LNA from 144 to 170 GHz ($V_d$ = 1.4 V, $I_{total}$ = 25 mA).

Fig. 8. Chip gain vs. input power level from -19 dBm to -4 dBm at 155-GHz ($V_d$ = 1,4 V, $I_{total}$ = 25 mA).

Fig. 9. Block diagram of the noise measurement test set up.

Fig. 10. Measured noise figure and associated gain (at chip) from 150 to 160 GHz at high gain bias condition ($V_d$ = 1.4 V, $I_{d1,2,3}$ = 10 mA).

## TABLES

Table 1. Measured noise figure and associated gain through the amplifier and waveguide test fixture of the 155-GHz LNA as a function of drain current in each stage (drain voltage fixed at 1.4 V). The numbers in the parenthesis are estimated chip performance accounting the 2.5 dB transition 1oss (2.5 dB added for gain and 1.25 dB subtracted for noise figure.) .

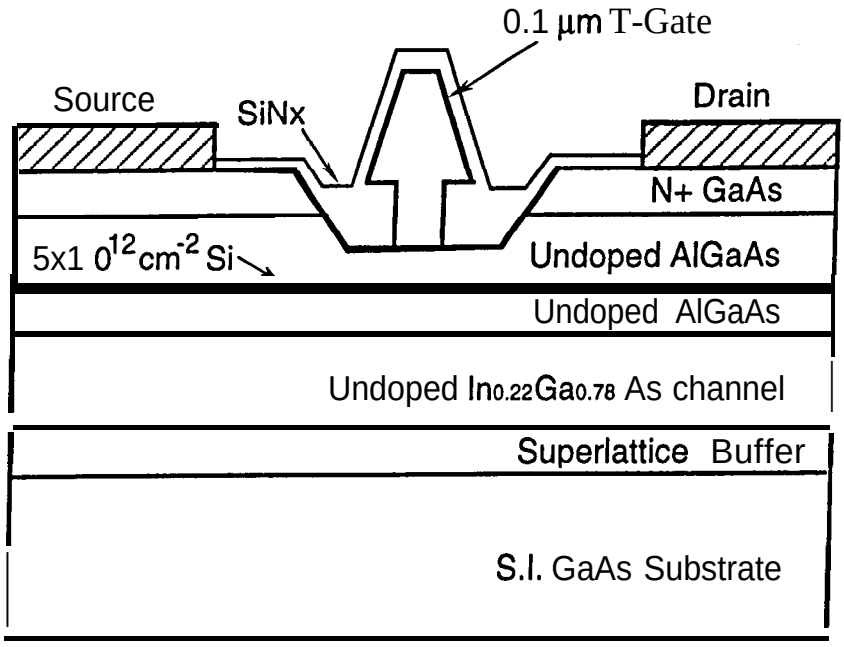
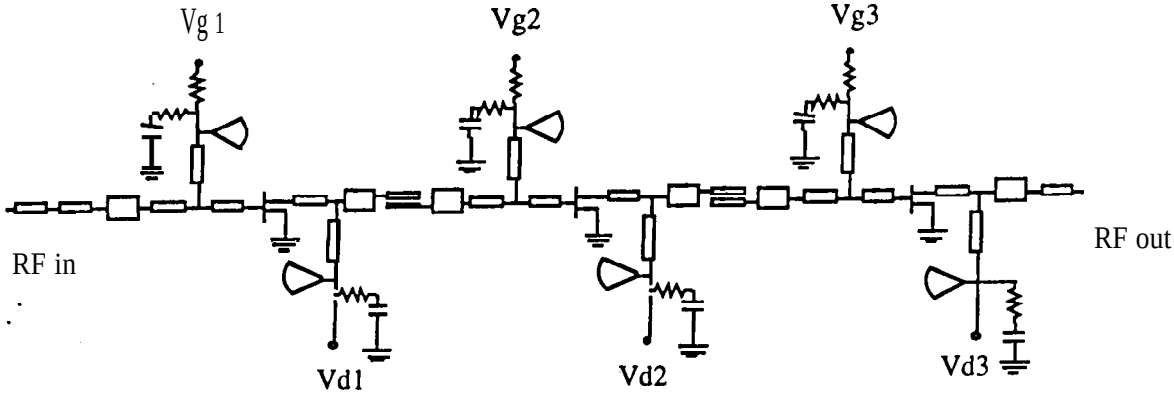
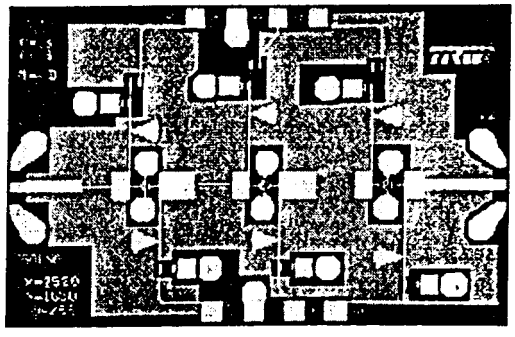

0.1 µm T-Gate
Source
SiNx
Drain
N+ GaAs
5x1 0^12cm^-2 Si
Undoped AlGaAs
Undoped AlGaAs
Undoped In0.22Ga0.78 As channel
Superlattice Buffer
S.I. GaAs Substrate

Fig. 1


Vg1
Vg2
Vg3
RF in
RF out
Vd1
Vd2
Vd3

(a)



(b)

Fig. 2

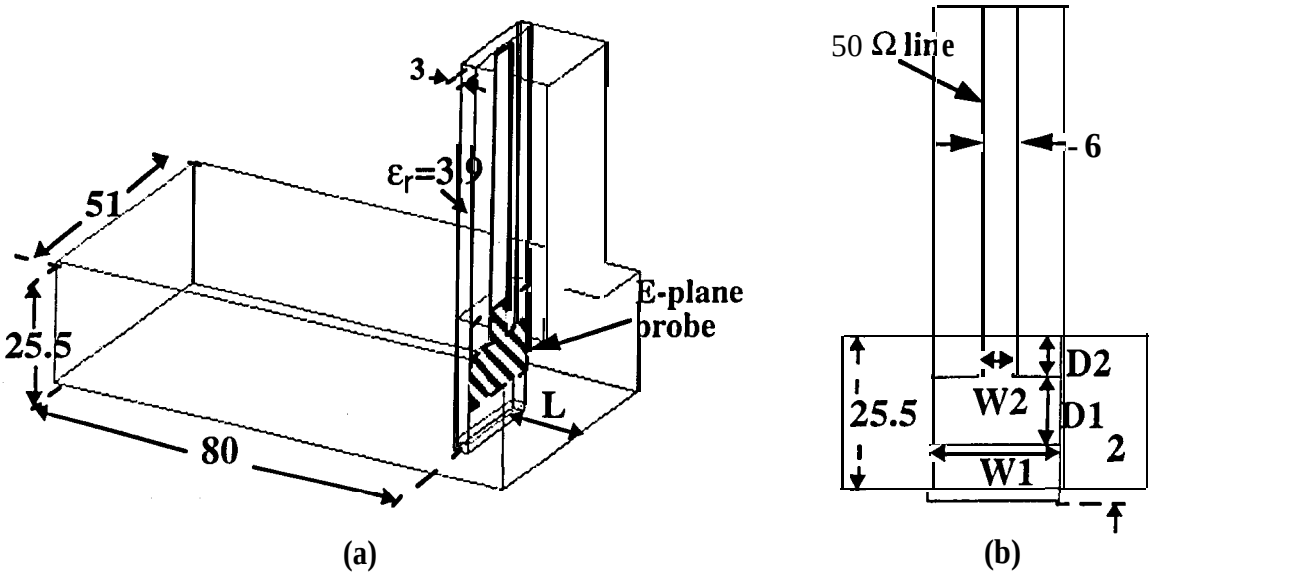

3
$\varepsilon_r$=3
51
25.5
80
L
E-plane
probe
(a)
50 Ω line
6
D2
W2
D1
25.5
W1
2
(b)

Fig. 3

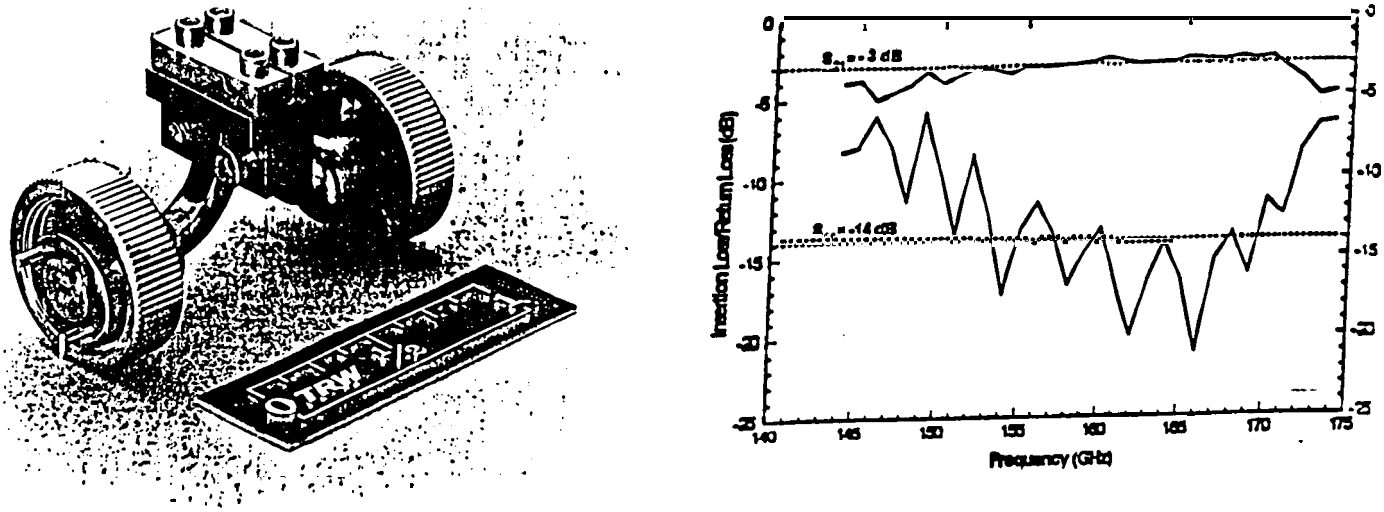

Insertion Loss/Return Loss (dB)
Frequency (GHz)
140
145
150
155
160
165
170
175
0
-5
-10
-15
-20
(a)
(b)

Fig. 4

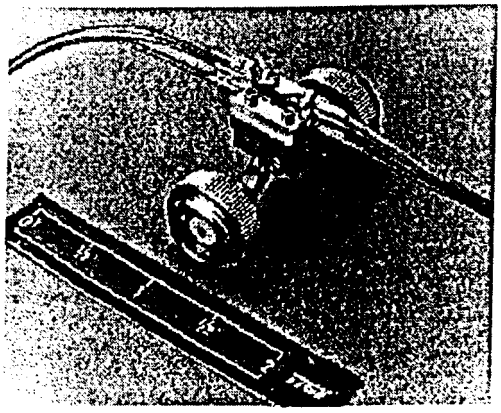


Fig. 5

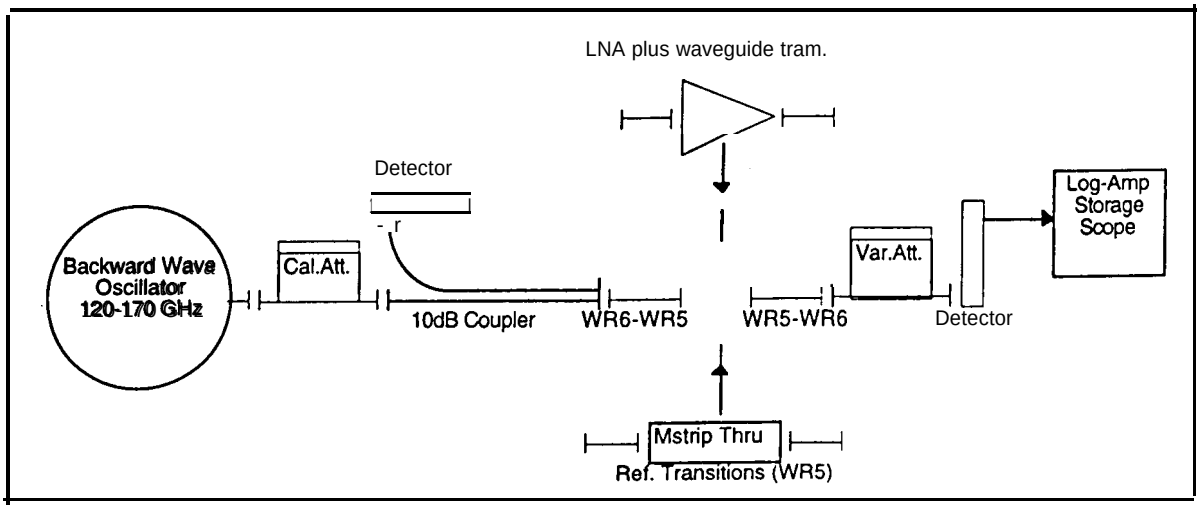

LNA plus waveguide tram.
Detector
Backward Wave
Oscillator
120-170 GHz
Cal.Att.
10dB Coupler
WR6-WR5
WR5-WR6
Var.Att.
Detector
Log-Amp
Storage
Scope
Mstrip Thru
Ref. Transitions (WR5)

Fig. 6

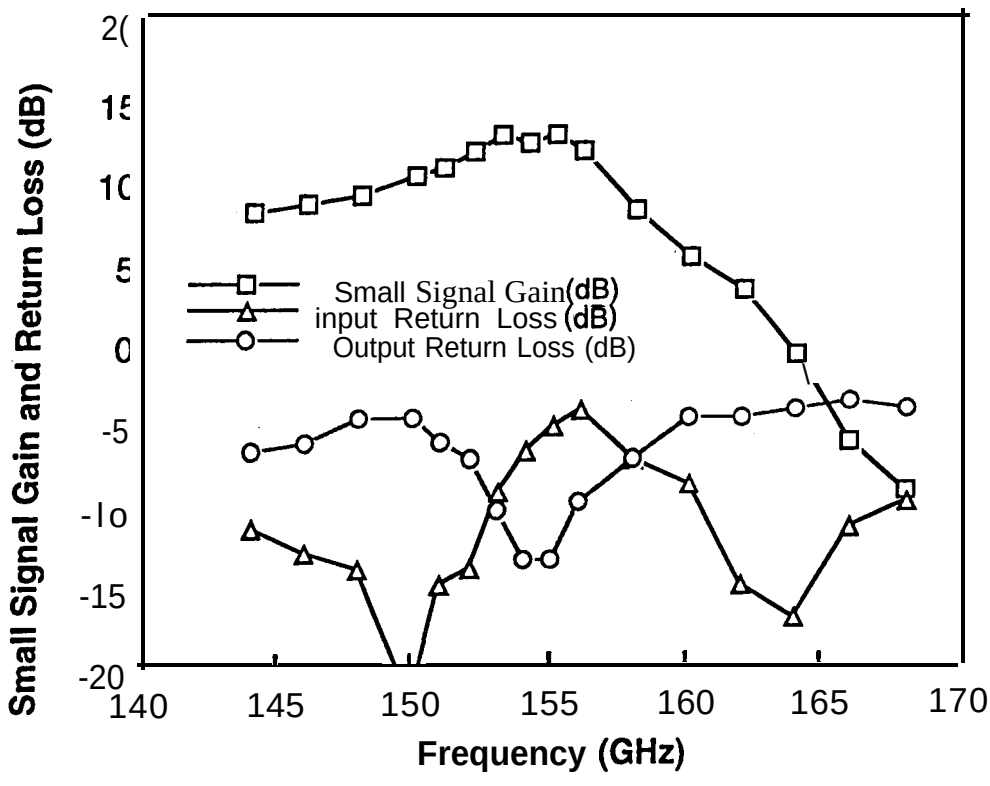

Small Signal Gain and Return Loss (dB)
2(
15
10
5
0
-5
-10
-15
-20
140
145
150
155
160
165
170
Frequency (GHz)
Small Signal Gain (dB)
input Return Loss (dB)
Output Return Loss (dB)

Fig. 7

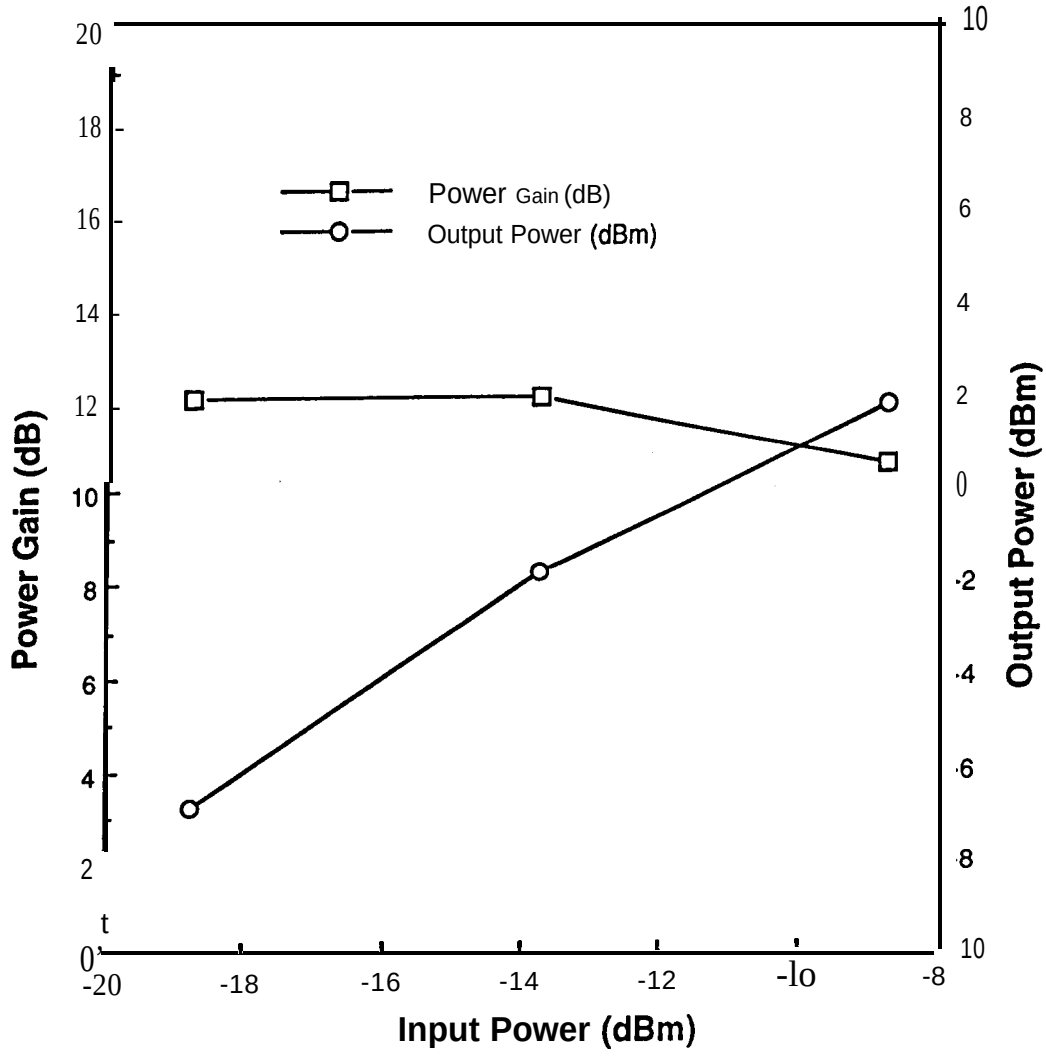

Power Gain (dB)
Output Power (dBm)
Power Gain (dB)
Output Power (dBm)
Input Power (dBm)
20
18
16
14
12
10
8
6
4
2
0
10
8
6
4
2
0
-2
-4
-6
-8
10
-20
-18
-16
-14
-12
-lo
-8

Fig. 8

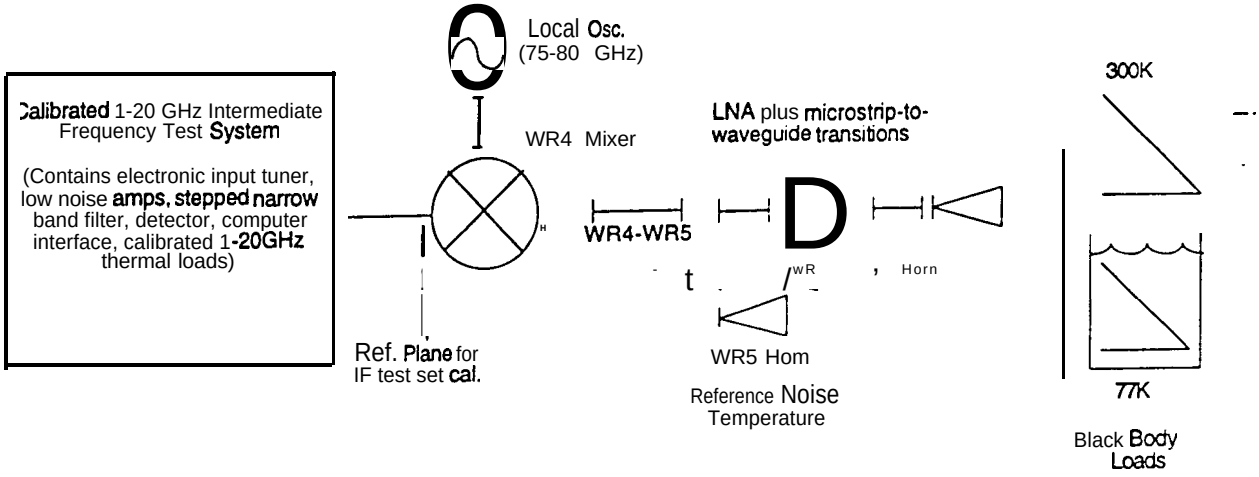

Calibrated 1-20 GHz Intermediate Frequency Test System
(Contains electronic input tuner, low noise amps, stepped narrow band filter, detector, computer interface, calibrated 1-20GHz thermal loads)
Local Osc.
(75-80 GHz)
WR4 Mixer
LNA plus microstrip-to-waveguide transitions
WR4-WR5
WR5 Horn
Ref. Plane for IF test set cal.
Reference Noise Temperature
300K
77K
Black Body Loads

Fig. 9

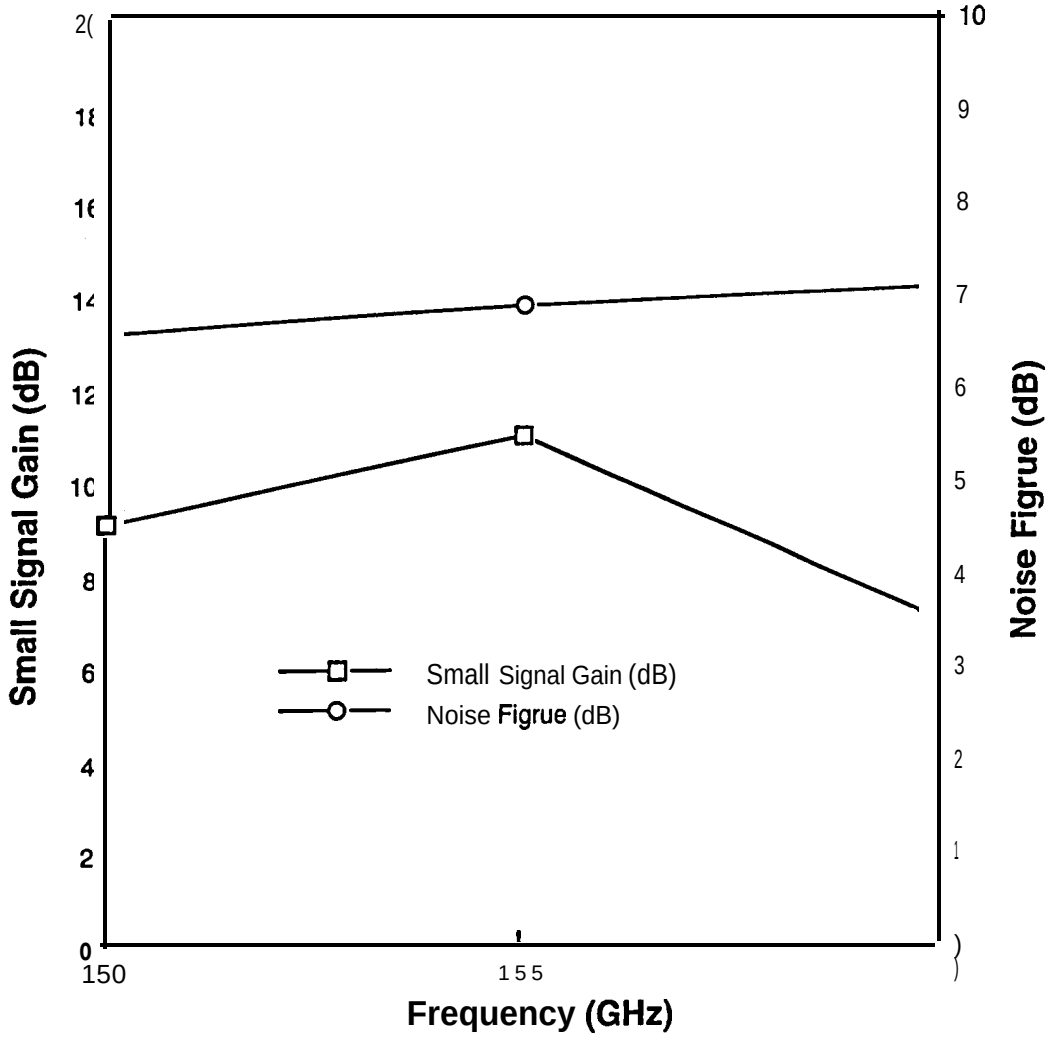

Small Signal Gain (dB)
Noise Figrue (dB)
Small Signal Gain (dB)
Noise Figrue (dB)
150
155
Frequency (GHz)

Fig. 10